PATENT

Attorney Docket No. MTI-31041-A

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Ping, et al.
Serial No.	:	10/046,497
Filing Date	:	October 26, 2001
For	:	Method For Forming Raised Structures by Controlled Selective Epitaxial Growth of Facet Using Spacer
Group Art Unit:		2814
Examiner	:	LE, Thao X.
Confirmation No.:		8624

CERTIFICATION OF SUBMISSION

I hereby certify that, on the date shown below, this correspondence is being transmitted via the Patent Electronic Filing System (EFS) addressed to Examiner LE at the U.S. Patent and Trademark Office.

Date: July 18, 2007

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Sir:

This is an appeal from the final rejection of Claims 143-148, 167-169, 173-175, 182-189, 197, 224, and 227-231 as stated in the Office Action mailed March 14, 2007. A Notice of Appeal was timely filed on May 14, 2007.

WHD\5213335.1

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There is a pending appeal for related application U.S. Serial No. 10/379,494 (Appeal Brief filed July 2, 2007).

Appellant's legal counsel: Kristine M. Strodthoff, Reg. No. 34,259, Whyte Hirschboeck Dudek S.C.

Assignee: Micron Technology, Inc.

III. STATUS OF CLAIMS

All the claims of this application and their individual status are reported in the Claims Appendix. Claims 143-148, 167-169, 173-175, 182-189, 197, 224, and 227-231 are on appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. <u>SUMMARY OF CLAIMED SUBJECT MATTER</u>

The independent claims under appeal are 143, 173, 182, 186, 197, 227, 229 and 230.

The claimed embodiment is described in the specification at page 4, line 18 to page 5, line 19, and at page 12, line 19 to page 14, line 6.

The claims under appeal are directed to the embodiment depicted in FIGS. 2A-2F, which illustrate a vertical structure (e.g., transistor) and raised adjacent structures (e.g., source/drain) with multiple epitaxial silicon layers, as shown below.

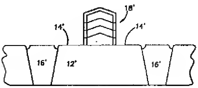


FIG.2E

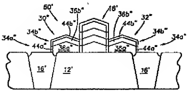
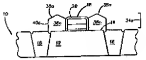
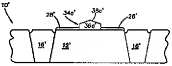
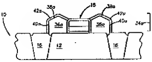
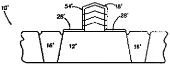
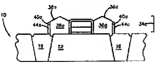
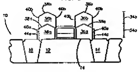
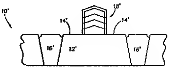
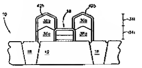
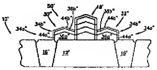


FIG.2F

Applicant's structures are distinguished from prior art structures by multiple and separate layers of epitaxially grown silicon, each layer having a top surface defined by multiple facets.

The multi-faceted top surface is the result of each silicon layer being epitaxially grown until facets are formed, whereupon the growth processed is stopped, an insulating layer is formed over the silicon layer, a portion of the insulating layer is removed to expose the top surface of the silicon layer, and then another silicon layer is epitaxially grown. Unlike prior art structures (such as described in the references cited by the Examiner), Applicant's structures are <u>not</u> formed within an opening in an insulating layer. Rather, Applicant's structures are epitaxially grown from the surface of a substrate in stages in a vertical orientation by forming an insulating layer on the sidewalls of each epitaxial layer to prevent lateral/horizontal growth of silicon from angled facets that form on the epitaxial layer.

As background, Applicant's process for forming the claimed structures is illustrated below, generally in FIGS. 1B-1F, with the claimed embodiment (species) in FIGS. 2A-2F.

	Sequence of Structure Formation (Applicant's Process)	Sequence of Structure Formation for claimed species embodiment
A first faceted epitaxial silicon layer 36a is grown;	 FIG.1B	 FIG.2C
A first insulative layer 42a is deposited over the first epitaxial layer;	 FIG.1C	 FIG.2D
The insulative layer 42a is removed from top surface 38a of the first epitaxial layer;	 FIG.1D	
A second faceted epitaxial silicon layer 36b is grown on the first epitaxial layer;	 FIG.1E	 FIG.2E
A second insulative layer 42b is deposited – with the formed structure now having two epitaxial layers.	 FIG.1F	 FIG.2F

Regarding the elements of Claim 143, the structure is vertically oriented and composed of at least two (multiple) overlying faceted layers of epitaxial silicon with each silicon layer having a faceted surface with a plurality of facets and sidewalls with an overlying insulative layer, and an uppermost faceted epitaxial silicon layer covered by an insulative layer, as described in the specification at page 4, line 18 to page 5, line 19, and at page 12, line 19 to page 14, line 6, with reference to FIGS. 2E and 2F (see above).

Regarding Claim 173, the elements are as stated for Claim 143, with the exception that the structure is defined as a component of a transistor, as described in the specification at page 4, line 20.

Regarding Claims 182, 186 and 197, the elements are as stated for Claim 143.

Regarding Claim 227, the elements are as stated for Claim 143, with the exception that the faceted surface of the first epitaxial silicon layer is defined as having a facet in a horizontal plane orientation, and the insulative spacer on the sidewalls but not on the horizontal plane-oriented facet of the first silicon layer, and the second epitaxial silicon layer is situated on the horizontal plane-oriented facet of the first silicon layer, as described in the specification at page 2, lines 24-26 and at page 3, lines 2-6 (and the originally-filed claims 48, 59, 59 and 72 of the parent application USSN 09/816,962, now U.S. Pat. No. 7,176,109).

Regarding Claim 229, the elements are as stated for Claim 227, with the exception that both epitaxial silicon layers have an upper faceted surface with a facet in a horizontal plane orientation, as described in the specification at page 2, lines 24-26, at page 3, lines 2-6, and at page 4, lines 6-14.

Regarding Claim 230, the elements are as stated for Claim 229, with the exception that the upper faceted surface of the epitaxial silicon layers is defined as having a plurality of facets in an angled plane orientation and a facet in a horizontal plane orientation, as described in the specification at page 9, lines 15-19, and at page 8, lines 22-26, and the figures (FIGS. 1B-1F and 2E-2F) (and the originally-filed claims 48, 59, 59 and 72 of the parent application USSN 09/816,962, now U.S. Pat. No. 7,176,109).

Regarding Claim 232, the elements are as stated for Claim 229, with the exception that the plane orientation of the facets are defined as being in a (110), (111) or (100) orientation, as described in the specification at page 8, lines 22-25, at page 9, lines 15-16, and at page 10, lines 15-17.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 143-144, 147, 167, 169, 173, 175, 182-189, 197 and 227-231 are unpatentable under 35 USC §§ 102(b)/103(a) as being anticipated by or obvious over Matsumoto (JP 401286361).

Whether Claims 145-146, 148, 168 and 174 are unpatentable under 35 USC §103(a) as being obvious over Matsumoto (JP 401286361) in view of Sharma (USP 5,483,094).

Whether the Examiner's withdrawal of Claims 149-155, 170-172, 176-181, 190-193, 196, 198-226 and 232 is proper.

VII. ARGUMENT

Whether Claims 143-144, 147, 167, 169, 173, 175, 182-189, 197 and 227-231 are unpatentable under 35 USC §§ 102(b)/103(a) as being anticipated by or obvious over Matsumoto (JP 401286361).

The Examiner rejected Claims 143-144, 147, 167, 169, 173, 175, 182-189, 197 and 227-231 are unpatentable under 35 USC §102(b) as being anticipated by Matsumoto (JP 401286361) (Office Action, March 14, 2007) The Examiner states that (emphasis added):

> Regarding Claims 143, 173, 182, 186, 197, 227, 229 and 230, Matsumoto discloses a semiconductor structure in fig. 3, comprising *at least two overlying faceted layers 4/6* of single crystal epitaxial silicon (ES), *each ES layer* comprising a faceted surface comprising a plurality of facets, fig. 3, and sidewalls with insulative materials 3 thereover, and an uppermost faceted layer of *at least two overlying layers of ES* having a layer of insulative material 5 over the faceted surface of uppermost layer of ES, where the structure is situated on a substrate 1 in a vertical orientation, fig. 3 and attached abstract and constitution.

In response to Applicant's arguments, the Examiner states that (emphasis added):

> Applicant's arguments filed Nov. 2, 2006 have been fully considered but they are not persuasive. The Applicant requests a written text in Matsumoto that describes a second SEG layer. *The fig. 3 of Masumoto <u>shows</u> two SEG layers 4 and 6. <u>No additional text is necessary</u>. <u>It is apparent that the Applicant's argument replies</u>* <u>[sic]</u> *<u>on the different method between Matsumoto and present invention</u>.* However, the patentability of a product does not depend on its method of production. *<u>If the product in a product-by-process claim</u>* is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."...

Applicant respectfully traverses.

First of all, contrary to the Examiner's assertion, Applicant does <u>not</u> rely on the method of production of its structures or compared that method to the process of Matsumoto. Applicant's structures themselves differ from Matsumoto's structures in the construction and elements, as discussed below, regardless of the method of production.

Matsumoto does not anticipate or make obvious the pending claims because Matsumoto does not disclose two distinct epitaxial (SEG) silicon layers. And contrary to the Examiner's statement, there *<u>is</u>* text in Matsumoto that describes the structure in the figures, which requires consideration for a proper construction of cited figure 3.

The text of Matsumoto in the Abstract clearly describes a *single* SEG layer – layer 4 in Fig. 3(b) (and in Fig. 1). The Abstract also states that the area designated as "6" is formed if *boron is implanted into layer 4.* Such boron implantation forms a doped uniform base 6 to the depth shown in Fig. 3(b) (and in Fig. 1) (emphasis added).

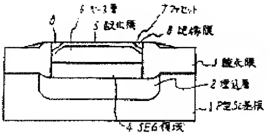


FIG. 1

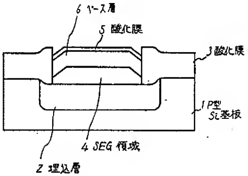


FIG. 3(b)

Abstract of JP1286361

PURPOSE: To arrange the constitution so that characteristic abnormality such as drop of withstand voltage of a device, etc., may not occur by providing an insulation film formed on the surface of a selected epitaxial layer by a rotary application method.

CONSTITUTION: As is doped to a P type silicon substrate 1 so as to form an N type buried layer 2 and an oxide film 3 is grown at the surface. A window is opened inside the buried layer 2, and a phosphorous doped N type SEG (selective epitaxial growth) area 4 is grown. *And an oxide film 5 is grown on the SEG area 4*. Next, an insulation film 8 is formed by a rotary application method. Since applied film is formed thick on a facet 7 at the corner part of the SEG area 4 this way and the entire surface of the SEG area 4 is planed, *if boron is implanted by an ion implanting method, uniform base 6 is formed*. Hereby, even if impurity is implanted by the ion implanting method, *an impurity introduced layer is formed uniformly to the depth direction inside the selective epitaxial layer*, therefore drop of withstand voltage does not occur.

Region 6 is not a second SEG layer. It is a depth of SEG layer 4 that is doped *after* layer 4 is formed. The "line" within the SEG layer 4 indicates the *depth* of the boron that is introduced into layer 4 to form boron-doped region 6.

The Examiner has ignored Matsumoto's description of doping SEG area 4 to form doped area 6, and incorrectly interpreted Fig. 3(b) of that reference.

Matsumoto discloses a single SEG layer 4. As such, Matsumoto does not anticipate or make obvious any of the pending claims of this application.

The Examiner has failed to properly show a case of either anticipation or a *prima facie* case of obviousness based on Matsumoto.

Whether Claims 145-146, 148, 168 and 174 are unpatentable under 35 USC §103(a) as being obvious over Matsumoto (JP 401286361) in view of Sharma (USP 5,483,094).

The Examiner rejected *dependent* Claims 145-146, 148, 168 and 174 under 35 USC §103(a) as obvious over Matsumoto (JP 401286361) in view of Sharma (USP 5,483,094).

Regarding claims 145-146 and 148, the Examiner cites Sharma for teaching an insulative layer 41/61 of silicon oxide and/or silicon nitride, and a dielectric layer having a thickness of about 5-20 nm or 2-5nm.

Regarding claims 168 and 174, the Examiner states that the recitation of "being a transistor gate" does not result in a structural difference, and that Matsumoto's structure is capable of being a transistor gate.

Applicant respectfully traverses.

For the reasons stated above regarding Matsumoto's failure to teach or suggest Applicant's structures/devices as claimed, the additional information from Sharma as to the thickness of a dielectric layer, does not overcome the failure of Matsumoto to teach a device having *multiple* overlying epitaxial silicon layers.

In sum, Matsumoto, either alone or in combination with Sharma, do *not* teach or suggest Applicant's structures as claimed. Accordingly, withdrawal of these rejections is respectfully requested.

For the reasons stated in the above arguments, Applicant believes that the claims on appeal comply with 35 U.S.C. §§ 102/103, and requests that the final rejection of the claims on appeal be reversed.

Whether the Examiner's withdrawal of Claims 149-155, 170-172, 176-181, 190-193, 196, 198-226 and 232 is proper.

In response to the Examiner request for restriction of species, Applicant elected Species subgroup "b" relating to FIGS. 2A-2F.

Applicant identified Claims 143, 173, 182, 186, 197, 227, 229 and 230 as generic. It is further submitted that Claim 225 is also generic.

Applicant listed Claims 143-155, 167-193 and 196-232 as readable thereon. However, of those claims, the Examiner has withdrawn Claims 149-155, 170-172, 176-181, 190-193, 196 and 198-226, as being drawn to an unelected species, stating as follows:

> 1. Applicant's election of Species Subgroup "b"; fig. 2A-2F corresponding generic claims 143, 173, 182, 186, 197, 227, 229 and 230 in the reply filed on 05 Jan. 2007 is acknowledged; thus claims 143-148, 167-169, 173-175, 182-189, 197, 224, 227-231 are being considered, while claims 149-155, 170-172, 176-181, 190-193, 196, 198-226, and 232 are withdrawn from consideration....

Applicant respectfully traverses.

The withdrawn independent claims are 149, 176, 179, 190, 196, 198-202 and 225, and product-by-process Claims 203 and 213-214.

Applicant submits that all of the listed withdrawn claims correspond to and include all of the limitations of the elected species FIGS. 2A-2F, which illustrate a vertical structure (e.g., transistor) and raised adjacent structures (e.g., source/drain) with multiple epitaxial silicon layers, as shown below.

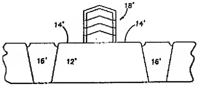


FIG.2E

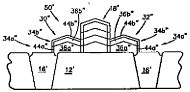


FIG.2F

Regarding withdrawn Claims 149, 190, 196, 198 and 202, the elements are as stated for Claim 143, with the exception that one or more silicon layer comprises a conductivity enhancing dopant, as described in the specification at page 5, lines 12-15.

Regarding withdrawn Claims 176 and 199, the elements are as stated for Claim 173.

WHD\5213335.1

Regarding withdrawn Claims 179 and 200, the elements are as stated for Claim 173, with the exception that one or more silicon layer comprises a conductivity enhancing dopant, as described in the specification at page 5, lines 12-15.

Regarding withdrawn Claim 201, the elements are as stated for Claim 143.

Regarding withdrawn Claims 204-212, the elements are as stated for Claim 143, with the exception that the process of forming the structure is additionally recited, as described in the specification at page 2, line 14 to page 3, line 12, at page 12, line 19 to page 14, line 6, and in FIGS. 2A-2F.

Regarding withdrawn Claim 203, the elements are as stated for withdrawn Claim 204, with the exception of exposing the top surface of the second layer and repeating the process steps, as described in the specification at page 4, lines 10-13, and at page 14, lines 1-3.

Regarding withdrawn Claims 213-214, the elements are as stated for withdrawn Claim 203, with the exception of doping the second silicon layer with a conductivity enhancing dopant, as described in the specification at page 4, lines 14-17, and at page 4, lines 4-6.

Regarding withdrawn Claims 215-223, the elements are as stated for Claim 143, with the exception that the process of forming the structure is additionally recited, including doping of the uppermost silicon layer, as described in the specification at page 4, lines 14-17, and at page 14, lines 4-6.

Regarding withdrawn Claim 225 to a raised structure, the elements are as stated for Claim 143, with the exception that the claim does not positively recite that the uppermost epitaxial silicon layer is covered by an insulative layer, as described in the specification at page 4, lines 6-10.

Each of the withdrawn claims includes the elements recited in the claims under consideration by the Examiner. Accordingly, reinstatement of the withdrawn claims is therefore proper.

Extension of Term.

The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

Respectfully submitted,

Kristine M Strodthoff

Dated: July 18, 2007

Kristine M. Strodthoff
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VIII. CLAIMS APPENDIX

1-142. (canceled)

143. (previously presented) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each epitaxial silicon layer comprising:

a faceted surface comprising a plurality of facets, and

sidewalls with insulative material thereover, and

an uppermost faceted layer of the at least two overlying layers of epitaxial silicon having a layer of an insulative material over the faceted surface of said uppermost layer of epitaxial silicon;

wherein the structure is situated on a substrate in a vertical orientation.

144. (previously presented) The semiconductor structure of Claim 143, wherein the insulative layer comprises an oxide film, a nitride film, an oxidized nitride film, or a composite oxide/nitride film.

145. (previously presented) The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon nitride film.

146. (previously presented) The semiconductor structure of Claim 145, wherein the silicon nitride film has a thickness of about 5 to about 20 nm.

147. (previously presented) The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon oxide film.

148. (previously presented) The semiconductor structure of Claim 147, wherein the silicon oxide film has a thickness of about 2 to about 5 nm.

149. (withdrawn) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of said layers comprising a faceted surface comprising a plurality of facets, sidewalls, and an insulative material over the sidewalls, an uppermost layer of the at least two overlying layers having a layer of an insulative material over the faceted surface; one or more of the layers of epitaxial silicon comprising a conductivity enhancing dopant; wherein the structure is situated on a substrate in a vertical orientation.

150. (withdrawn) The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises a p-type dopant.

151. (withdrawn) The semiconductor structure of Claim 150, wherein the p-type dopant is selected from the group consisting of diborane, boron trichloride, and boron trifluoride, and combinations thereof.

152. (withdrawn) The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises an n-type dopant.

153. (withdrawn) The semiconductor structure of Claim 152, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

154. (withdrawn) The semiconductor structure of Claim 149, wherein one or more of the layers of epitaxial silicon comprises a concentration gradient of the dopant.

155. (withdrawn) The semiconductor structure of Claim 154, wherein the concentration gradient comprises a low to high concentration of the dopant within the one or more of the layers of epitaxial silicon, with the high dopant concentration at the surface of said one or more of the layers.

156-166. (canceled)

167. (previously presented) The semiconductor structure of Claim 143, being a component of a transistor.

168. (previously presented) The semiconductor structure of Claim 167, being a transistor gate.

169. (previously presented) The semiconductor structure of Claim 167, being a source/drain diffusion region.

170. (withdrawn) The semiconductor structure of Claim 149, being a component of a transistor.

171. (withdrawn) The semiconductor structure of Claim 170, being a transistor gate.

172. (withdrawn) The semiconductor structure of Claim 170, being a source/drain diffusion region.

173. (previously presented) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon; each of said faceted layers comprising a faceted top surface comprising a plurality of facets, and insulated sidewalls, and the uppermost faceted layer of epitaxial silicon having an insulated top surface; the structure situated on a substrate in a vertical orientation; the structure being a component of a transistor.

174. (previously presented) The semiconductor structure of Claim 173, being a transistor gate.

175. (previously presented) The semiconductor structure of Claim 173, being a source/drain diffusion region.

176. (withdrawn) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers comprising a faceted top surface comprising a plurality of facets, sidewalls, and

insulative material over the sidewalls, an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers having a layer of an insulative material over the top surface; the structure situated on a substrate in a vertical orientation; the structure being a component of a transistor.

177. (withdrawn) The semiconductor structure of Claim 176, being a transistor gate.

178. (withdrawn) The semiconductor structure of Claim 176, being a source/drain diffusion region.

179. (withdrawn) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers comprising a faceted top surface comprising a plurality of facets, sidewalls, and insulative material over the sidewalls, an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers having a layer of an insulative material over the top surface; one or more of the at least two overlying faceted layers of epitaxial silicon comprising a conductivity enhancing dopant; the structure situated on a substrate in a vertical orientation; and the structure being a component of a transistor.

180. (withdrawn) The semiconductor structure of Claim 179, being a transistor gate.

181. (withdrawn) The semiconductor structure of Claim 179, being a source/drain diffusion region.

182. (previously presented) A semiconductor device, comprising:

a structure comprising at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon comprising a faceted top surface comprising a plurality of facets, and insulated sidewalls, and an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers of epitaxial silicon having an insulated top surface; the structure situated on a substrate in a vertical orientation.

183. (previously presented) The semiconductor device of Claim 182, comprising a transistor.

184. (previously presented) The semiconductor device of Claim 183, wherein the structure comprises a transistor gate.

185. (previously presented) The semiconductor device of Claim 183, wherein the structure comprises a source/drain diffusion region.

186. (previously presented) A semiconductor device, comprising:

a structure comprising at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon comprising a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material over the sidewalls; an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers of epitaxial silicon having a layer of an insulative material over the top surface; and the structure situated on a substrate in a vertical orientation.

187. (previously presented) The semiconductor device of Claim 186, comprising a transistor.

188. (previously presented) The semiconductor device of Claim 187, wherein the structure comprises a transistor gate.

189. (previously presented) The semiconductor device of Claim 187, wherein the structure comprises a source/drain diffusion region.

190. (withdrawn) A semiconductor device, comprising:

a structure comprising at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon comprising a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material over the sidewalls; an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers of epitaxial silicon having a layer of an insulative material over the top surface; one or more of the

at least two faceted layers of epitaxial silicon comprising a conductivity enhancing dopant; and the structure situated on a substrate in a vertical orientation.

191. (withdrawn) The semiconductor device of Claim 190, comprising a transistor.

192. (withdrawn) The semiconductor device of Claim 191, wherein the structure comprises a transistor gate.

193. (withdrawn) The semiconductor device of Claim 191, wherein the structure comprises a source/drain diffusion region.

194-195. (canceled)

196. (withdrawn) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of the at least two faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, sidewalls, and insulative spacers over the sidewalls, an uppermost faceted layer of epitaxial silicon having a layer of an insulative material over the top surface; one or more of the at least two layers of epitaxial silicon comprising a conductivity enhancing dopant; and the structure situated on a substrate in a vertical orientation.

197. (previously presented) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon comprising a faceted top surface comprising a plurality of facets, sidewalls, and insulative material along the sidewalls, an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers having a layer of an insulative material over the top surface of said uppermost faceted layer; and the structure situated on a substrate in a vertical orientation.

198. (withdrawn) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon comprising a faceted top surface comprising a plurality of facets, and insulated sidewalls; an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers having a layer of an insulative material over the top surface of said uppermost faceted layer; one or more of the faceted layers of epitaxial silicon comprising a conductivity enhancing dopant; and the structure situated on a substrate in a vertical orientation.

199. (withdrawn) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, sidewalls, and insulative spacers over the sidewalls; an uppermost faceted layer of epitaxial silicon having a layer of an insulative material over the top surface of said uppermost faceted layer; the structure situated on a substrate in a vertical orientation; the structure being a component of a transistor.

200. (withdrawn) A semiconductor structure, comprising:

at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, sidewalls, and insulative spacers over the sidewalls; an uppermost faceted layer of epitaxial silicon having a layer of an insulative material over the top surface of said uppermost faceted layer; one or more of the at least two overlying faceted layers of epitaxial silicon comprising a conductivity enhancing dopant; the structure situated on a substrate in a vertical orientation; and the structure being a component of a transistor.

201. (withdrawn) A semiconductor device, comprising:

a structure comprising at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and insulated sidewalls, an uppermost faceted layer of epitaxial silicon of the at least two overlying faceted layers of epitaxial silicon having a layer of an insulative material

over the top surface of said uppermost faceted layer; and the structure situated on a substrate in a vertical orientation.

202. (withdrawn) A semiconductor device, comprising:

a structure comprising at least two overlying faceted layers of single crystal epitaxial silicon, each of said faceted layers of epitaxial silicon comprising a faceted top surface comprising a plurality of facets, and sidewalls covered by an insulative material; an uppermost faceted layer of epitaxial silicon of the at least two overlying epitaxial silicon faceted layers having a layer of an insulative material over the top surface of said uppermost faceted layer; one or more of the faceted layers of epitaxial silicon comprising a conductivity enhancing dopant; and the structure situated on a substrate in a vertical orientation.

203. (withdrawn) A semiconductor structure on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon on the substrate; the first faceted layer of epitaxial silicon comprising sidewalls and a faceted top surface comprising a plurality of facets;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first faceted layer of epitaxial silicon;

selectively growing a second faceted layer of epitaxial silicon on the exposed top surface of the first faceted layer of epitaxial silicon, the second faceted layer of epitaxial silicon comprising sidewalls and a faceted top surface comprising a plurality of facets; and

depositing an insulative material layer thereover.

204. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost layer; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first faceted layer of epitaxial silicon;

selectively growing a second faceted layer of epitaxial silicon on the exposed top surface of the first faceted layer of epitaxial silicon;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second faceted layer of epitaxial silicon;

repeating the steps of selectively growing a faceted layer of epitaxial silicon, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein, upon selectively growing the uppermost faceted layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost faceted layer of epitaxial silicon.

205. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost layer; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each faceted layer of epitaxial silicon, depositing an insulative film over the underlying layers of epitaxial silicon, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the epitaxial silicon on the exposed top surface of said preceding layer of epitaxial silicon to form a faceted layer of epitaxial silicon; and,

upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

206. (withdrawn) A stacked, vertically oriented semiconductor structure on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon crystal; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost faceted layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each faceted layer of epitaxial silicon, depositing an oxide film and removing a portion of the oxide film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the faceted layer of epitaxial silicon on the exposed top surface of said preceding layer of epitaxial silicon; and,

upon selectively growing the uppermost faceted layer of epitaxial silicon, depositing an oxide film layer thereover, with no subsequent removal of the oxide film layer from the top surface of said uppermost faceted layer of epitaxial silicon.

207. (withdrawn) A stacked, vertically oriented semiconductor structure on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost faceted layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each faceted layer of epitaxial silicon, depositing a nitride film and removing a portion of the nitride film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the faceted layer of epitaxial silicon on the exposed top surface of said preceding layer; and,

upon selectively growing the uppermost layer of epitaxial silicon, depositing a nitride film layer thereover, with no subsequent removal of the nitride film layer from the top surface of said uppermost layer of epitaxial silicon.

208. (withdrawn) A stacked, vertically oriented semiconductor structure on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost faceted layer of epitaxial silicon comprises an insulative film on the top surface of said layer; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate to about 450°C to about 950°C., and flowing at least one silicon precursor gas over the substrate at a rate of about 10 sccm to about 500 sccm, for about 15 seconds to about 30 seconds to form a faceted layer of epitaxial silicon;

wherein, prior to selectively growing each faceted layer of epitaxial silicon, depositing an insulative film over the underlying layers, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the faceted layer of epitaxial silicon on the exposed top surface of said preceding layer of epitaxial silicon; and,

upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

209. (withdrawn) A stacked, vertically oriented semiconductor structure on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial silicon crystal at about 20 nm/minute to about 40 nm/minute such that a faceted layer of epitaxial silicon is formed;

wherein, prior to selectively growing each layer of epitaxial silicon, depositing an insulative film over the underlying layers of epitaxial silicon, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the faceted layer of epitaxial silicon on the exposed top surface of said preceding layer of epitaxial silicon; and,

upon selectively growing the uppermost layer of epitaxial silicon depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

210. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of single crystal epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial silicon of less than about 10 nm/minute such that a faceted layer of epitaxial silicon is formed;

wherein, prior to selectively growing each layer of epitaxial silicon, depositing an insulative film over the underlying layers of epitaxial silicon, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the faceted layer of epitaxial silicon on the exposed top surface of said preceding layer of epitaxial silicon; and

upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

211. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost layers of single crystal epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the faceted layer of epitaxial silicon on the exposed top surface of said preceding layer of epitaxial silicon; and,

upon selectively growing the uppermost layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

212. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal nitridation, removing a portion of the

insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the layer of epitaxial silicon on the exposed top surface of said preceding layer of epitaxial silicon; and,

upon selectively growing the uppermost layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

213. (withdrawn) A semiconductor structure situated on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon on the substrate; the first layer of epitaxial silicon comprising sidewalls and a faceted top surface comprising a plurality of facets;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first layer of epitaxial silicon;

selectively growing a second faceted layer of epitaxial silicon on the exposed top surface of the first layer of epitaxial silicon while depositing a conductivity enhancing dopant, the second layer of epitaxial silicon comprising sidewalls and a faceted top surface comprising a plurality of facets;

depositing an insulative material layer thereover.

214. (withdrawn) A semiconductor structure situated on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of epitaxial silicon on the substrate; the first layer of epitaxial silicon comprising sidewalls and a faceted top surface comprising a plurality of facets;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first layer of epitaxial silicon;

selectively growing a second faceted layer of epitaxial silicon on the exposed top surface of the first layer of epitaxial silicon, the second layer of epitaxial silicon comprising sidewalls and a faceted top surface comprising a plurality of facets;

doping the second layer of epitaxial silicon with a conductivity enhancing dopant by ion implantation, and

depositing an insulative material layer thereover.

215. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial silicon crystal at about 20 nm/minute to about 40 nm/minute such that a faceted layer of epitaxial silicon is formed, wherein selectively growing at least the uppermost layer of epitaxial silicon comprises flowing the at least one silicon precursor gas with a conductivity enhancing dopant over the substrate; and

prior to selectively growing each layer of epitaxial silicon, depositing an insulative film over the underlying layers of epitaxial silicon, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the layer of epitaxial silicon on the exposed top surface of the preceding layer of epitaxial silicon; and,

upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

216. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost layer of epitaxial silicon; each of said faceted layers of epitaxial silicon

having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost faceted layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of said first layer of epitaxial silicon;

selectively growing a second faceted layer of single epitaxial silicon on the exposed top surface of said first layer of epitaxial silicon;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of said second layer of epitaxial silicon; and

repeating the steps of selectively growing a faceted layer of single crystal epitaxial silicon, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost faceted layer of epitaxial silicon, depositing a conductivity enhancing dopant to form a concentration of the dopant within said uppermost layer;

wherein, upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

217. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon;

selectively growing a second faceted layer of single crystal epitaxial silicon on the exposed top surface of the first layer of epitaxial silicon;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon; and

repeating the steps of selectively growing a faceted layer of single crystal epitaxial silicon, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost layer of epitaxial silicon, depositing a conductivity enhancing dopant at a variable rate to provide a concentration gradient of the dopant within the uppermost layer of epitaxial silicon;

wherein, upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

218. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon;

selectively growing a second faceted layer of single crystal epitaxial silicon on the exposed top surface of the first layer of epitaxial silicon;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon; and

repeating the steps of selectively growing a faceted layer of epitaxial silicon, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked

structure; and during the step of selectively growing the uppermost e layer of epitaxial silicon, depositing a conductivity enhancing dopant at an increasing rate over time to provide a low to high concentration of the dopant within the uppermost layer of epitaxial silicon;

wherein, upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

219. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon;

selectively growing a second faceted layer of single crystal epitaxial silicon on the exposed top surface of the first faceted layer of epitaxial silicon;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon; and

repeating the steps of selectively growing a faceted layer of single crystal epitaxial silicon, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein the uppermost layer of epitaxial silicon is selectively grown while doping, and upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

220. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon

including an uppermost faceted layer of single crystal epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon;

selectively growing a second faceted layer of single crystal epitaxial silicon on the exposed top surface of the first layer of epitaxial silicon;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon; and

repeating the steps of selectively growing a faceted layer of single crystal epitaxial silicon, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure;

wherein, upon selectively growing the uppermost layer of epitaxial silicon, doping the uppermost layer of epitaxial silicon with a conductivity enhancing dopant by ion implantation, and depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

221. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the faceted layer of epitaxial silicon on the exposed top surface of the preceding layer of epitaxial silicon; and, during the step of selectively growing the uppermost layer of epitaxial silicon, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost layer of epitaxial silicon; and

upon selectively growing the uppermost layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

222. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying faceted layers of single crystal epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding layer of epitaxial silicon, and selectively growing the layer of epitaxial silicon on the exposed top surface of the preceding layer of epitaxial silicon; and, during the step of selectively growing the uppermost layer of epitaxial silicon, depositing a conductivity enhancing dopant to form a concentration of the dopant within said uppermost layer of epitaxial silicon; and

upon selectively growing the uppermost layer of epitaxial silicon, forming an insulative film over the layers of epitaxial silicon by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

223. (withdrawn) A stacked, vertically oriented semiconductor structure situated on a substrate, the structure comprising overlying faceted layers of single crystal epitaxial silicon including an uppermost faceted layer of epitaxial silicon; each of said faceted layers of epitaxial silicon having a faceted top surface comprising a plurality of facets, and sidewalls, and insulative material on the sidewalls, and the uppermost layer of epitaxial silicon comprises an insulative film on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first faceted layer of single crystal epitaxial silicon on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first layer of epitaxial silicon;

selectively growing a second faceted layer of single crystal epitaxial silicon on the exposed top surface of the first layer of epitaxial silicon;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second layer of epitaxial silicon; and

repeating the steps of selectively growing a faceted layer of single crystal epitaxial silicon, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost layer of epitaxial silicon, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost layer of epitaxial silicon;

wherein, upon selectively growing the uppermost layer of epitaxial silicon, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost layer of epitaxial silicon.

224. (withdrawn) The semiconductor structure of Claim 143, wherein each of the faceted top surfaces of said faceted layers of epitaxial silicon defines a facet having a (100) plane orientation.

225. (withdrawn) A raised structure on a substrate, comprising a plurality of overlying layers of epitaxial silicon, each of said silicon layers having an upper surface comprising a plurality of facets, and sidewalls with an insulative layer thereover.

226. (withdrawn) The structure of Claim 225, wherein an uppermost silicon layer comprises a conductivity enhancing dopant.

227. (previously presented) A raised structure on a substrate, comprising:

a first layer of epitaxial silicon situated on the substrate, and comprising vertical sidewalls and an upper surface defining a plurality of facets including a facet in a horizontal plane orientation, with an insulative spacer overlying the sidewalls and the upper surface but not the horizontal plane oriented facet; and

a second layer of epitaxial silicon situated on the horizontal plane oriented facet of the upper surface of the first epitaxial silicon layer, and comprising vertical sidewalls and an upper surface, with an insulative spacer overlying the sidewalls and the upper surface.

228. (previously presented) The raised structure of Claim 227, wherein the upper surface of the second epitaxial silicon layer defines a plurality of facets.

229. (previously presented) A raised structure on a substrate, comprising:

at least two overlying layers of epitaxial silicon, including an uppermost epitaxial silicon layer, each epitaxial silicon layer having vertical sidewalls, and an upper surface defining a plurality of facets including a facet in a horizontal plane orientation; and

an insulative spacer overlying the sidewalls and the upper surface but not the horizontal plane oriented facet of the epitaxial silicon layers, with an insulative layer overlying the horizontal plane oriented facet of the upper surface of the uppermost epitaxial silicon layer.

230. (previously presented) A raised structure on a substrate, comprising:

at least two overlying layers of epitaxial silicon, including an uppermost epitaxial silicon layer, each epitaxial silicon layer having vertical sidewalls, and an upper surface defining a plurality of facets in an angled plane orientation and a facet in a horizontal plane orientation;

an insulative spacer overlying the sidewalls and the angled plane oriented facets but not the horizontal plane oriented facet; and

an insulative layer overlying the horizontal plane oriented facet of the upper surface of the uppermost epitaxial silicon layer.

231. (previously presented) The transistor of Claim 230, wherein an uppermost silicon layer comprises a conductivity enhancing dopant.

232. (withdrawn) A raised structure on a substrate, comprising:

at least two overlying layers of epitaxial silicon, including an uppermost epitaxial silicon layer, each epitaxial silicon layer having vertical sidewalls, and an upper surface defining a plurality of facets in a (110) or (111) plane orientation and a facet in a (100) plane orientation;

an insulative spacer overlying the sidewalls and the (110) or (111) plane oriented facets but not the (100) plane oriented facet; and

an insulative layer overlying the (100) plane oriented facet of the upper surface of the uppermost epitaxial silicon layer.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None. No decision has been rendered in the pending related appeal for U.S. Serial No. 10/379,494 (Appeal Brief filed July 2, 2007).